

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Inter Patent Application of  
NEVILL et al.

Atty. Ref.: 550-192

Serial No. 09/731,060

TC/A.U.: 2122

Filed: December 7, 2000

Examiner: Nguyen, A.

For: SCHEDULING CONTROL WITHIN A SYSTEM HAVING MIXED  
HARDWARE AND SOFTWARE BASED INSTRUCTION EXECUTION

\* \* \* \* \*

June 7, 2004

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Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Technology Center 2100

Sir:

**INFORMATION DISCLOSURE STATEMENT**

As suggested by 37 C.F.R. 1.97, the undersigned attorney brings to the attention of the Patent and Trademark Office the references listed on the attached form PTO-1449, a copy of each of which is enclosed. This is not to be construed as a representation that a search has been made or that no better prior art exists, or that a reference is relevant merely because cited.

The Examiner is requested to initial the attached form PTO-1449 and to return a copy of the initialed document to the undersigned as an indication that the attached references have been considered and made of record.

The requisite fee of \$180.00 to is included.

06/09/2004 MAHRED1 00000087 09731060

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180.00 DP

Respectfully submitted,

**NIXON & VANDERHYE P.C.**

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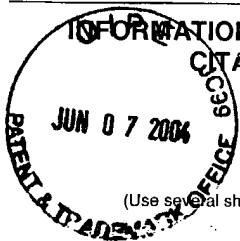
[illegible][illegible]

	IBM Technical Disclosure Bulletin, March 1988, pp 308-309, "System/370 Emulator Assist Processor For a Reduced Instruction Set Computer".
	IBM Technical Disclosure Bulletin, July 1986, pp 548-549, "Full Function Series/1 Instruction Set Emulator".
	IBM Technical Disclosure Bulletin, March 1994, pp 605-606, "Real-Time CISC Architecture HW Emulator On A RISC Processor".
	IBM Technical Disclosure Bulletin, March 1998, p272, "Performance Improvement Using An EMULATION Control Block".
	IBM Technical Disclosure Bulletin, January 1995, pp537-540, "Fast Instruction Decode For Code Emulation on Reduced Instruction Set Computer/Cycles Systems".
	IBM Technical Disclosure Bulletin, February 1993, pp231-234, "High Performance Dual Architecture Processor".

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

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INFORMATION DISCLOSURE  
CITATION

(Use several sheets if necessary)

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550-192

APPLICANT

NEVILL et al.

FILING DATE

December 7, 2000

SERIAL NO.

09/731,060

TC/A.U.

2122

	IBM Technical Disclosure Bulletin, August 1989, pp40-43, "System/370 I/O Channel Program Channel Command Word Prefetch".
	IBM Technical Disclosure Bulletin, June 1985, pp305-306, "Fully Microcode-Controlled Emulation Architecture".
	IBM Technical Disclosure Bulletin, March 1972, pp3074-3076, "Op Code and Status Handling For Emulation".
	IBM Technical Disclosure Bulletin, August 1982, pp954-956, "On-Chip Microcoding of a Microprocessor With Most Frequently Used Instructions of Large System and Primitives Suitable for Coding Remaining Instructions".
	IBM Technical Disclosure Bulletin, April 1983, pp5576-5577, "Emulation Instruction".
	Excerpts from the book ARM System Architecture by S. Furber.
	Excerpts from the book Computer Architecture: A Quantitative Approach by Hennessy et al.
	Excerpts from the book The Java Virtual Machine Specification by Tim Lindholm et al., 1 <sup>st</sup> and 2 <sup>nd</sup> editions.

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